REPLACEMENT SHEET
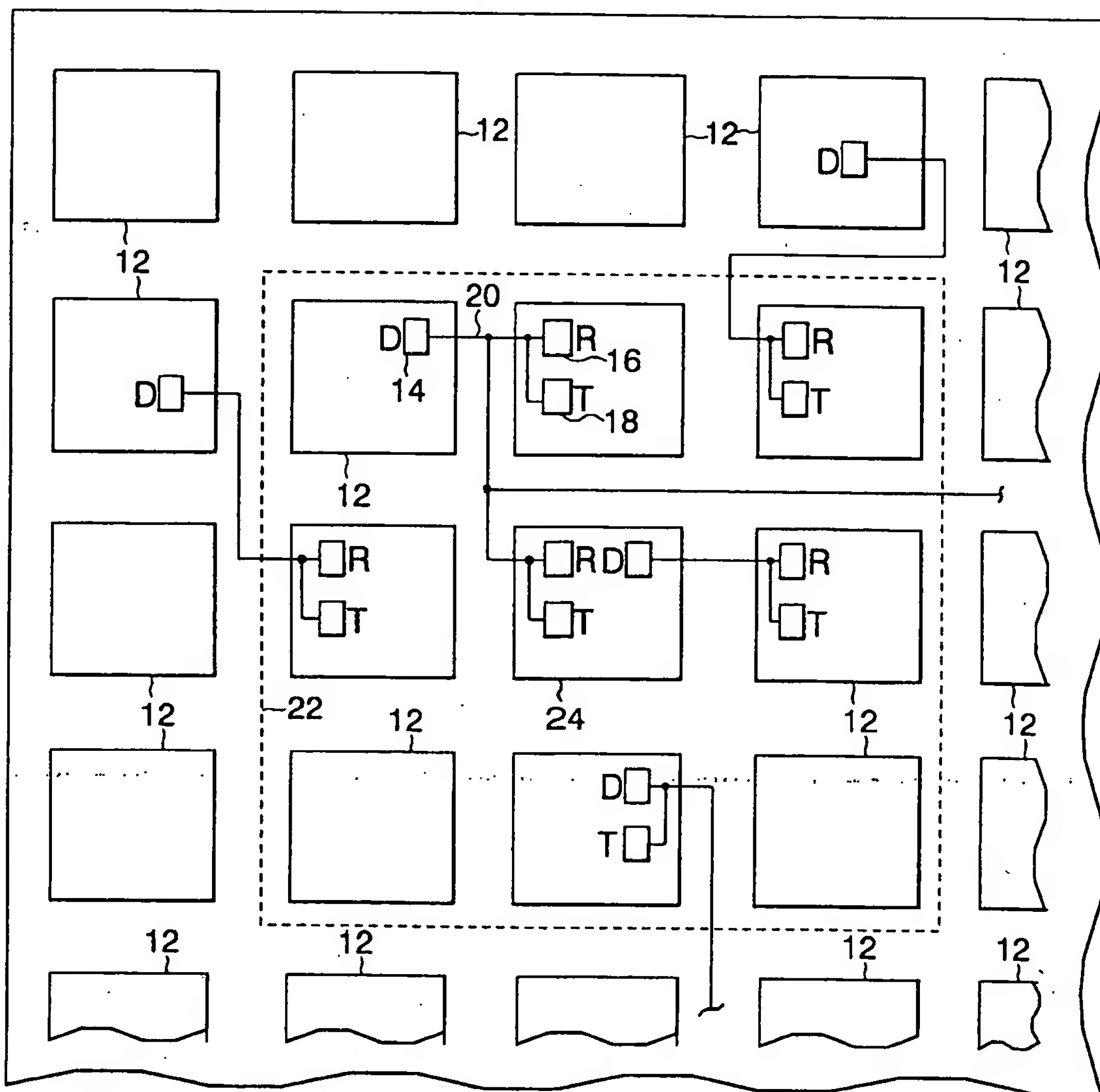
Kerry Bernstein, et al.
(RAH) BUR920010207US1
1/4

Reviewed
OK
2-26-05

10

(Prior Art)

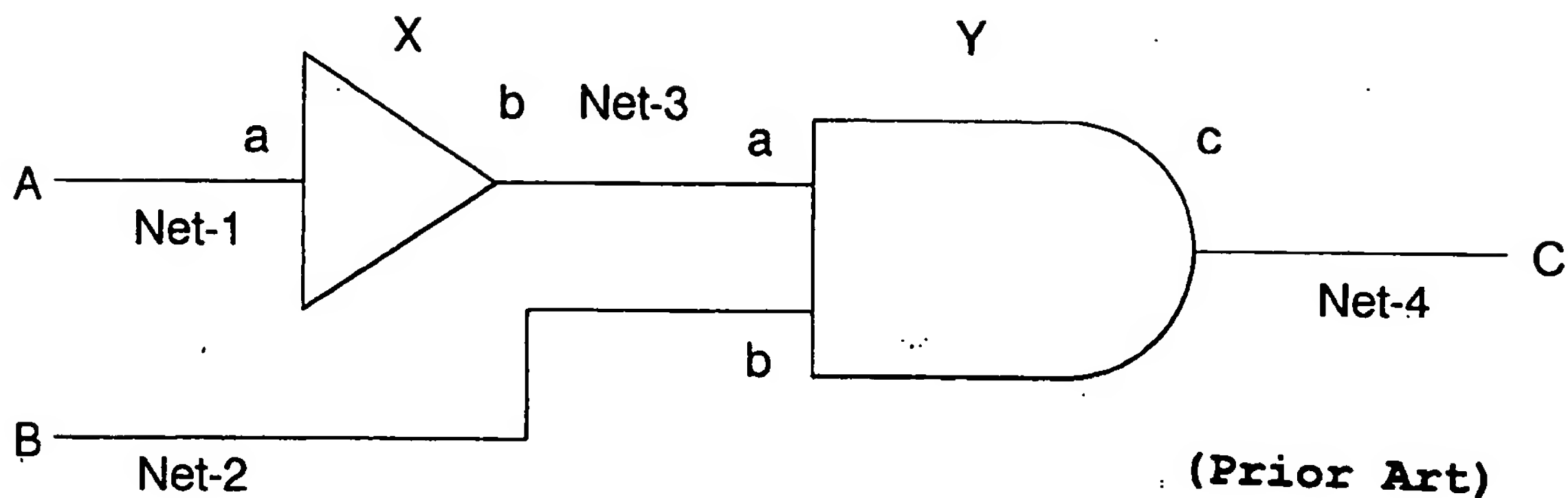# Figure 1

REVIEWED

OK
ger

2-26-05

EXAMPLE OF LOGIC CIRCUIT

(Prior Art)

Figure 2


```
Port:
  INPUT : A, B:
  OUTPUT: C
EndPort
Net:
  Net-1: pA, Xpa;
  Net-2: pB, Ypb;
  Net-3: Xpb, Ypa;
  Net-4; pC, Ypc;
EndNet;
```

(Prior Art)

EXAMPLE OF NET LIST

Figure 3

Reviewed "OK"

Jkh
1-6-04

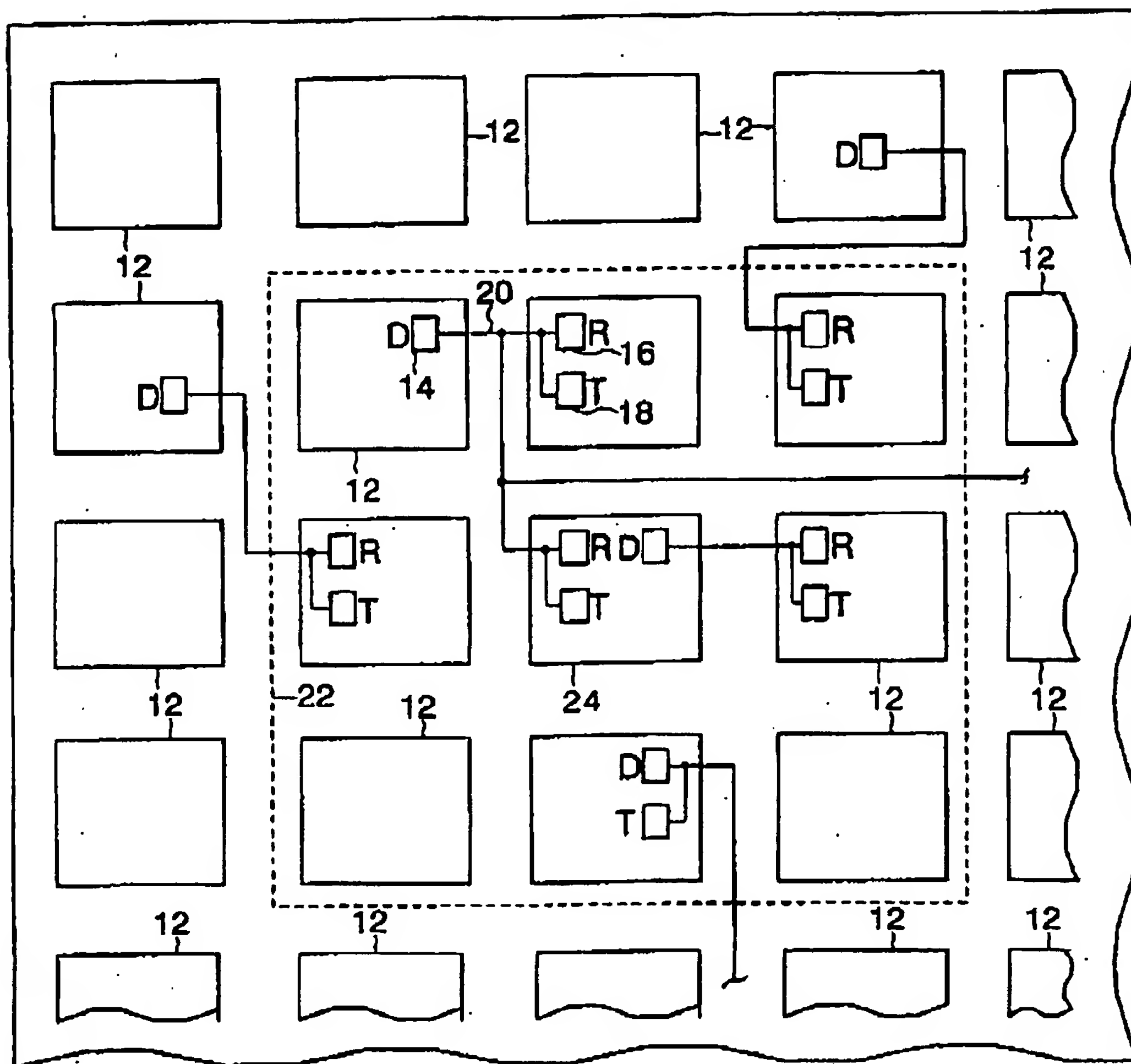Kerry Bernstein, et al.
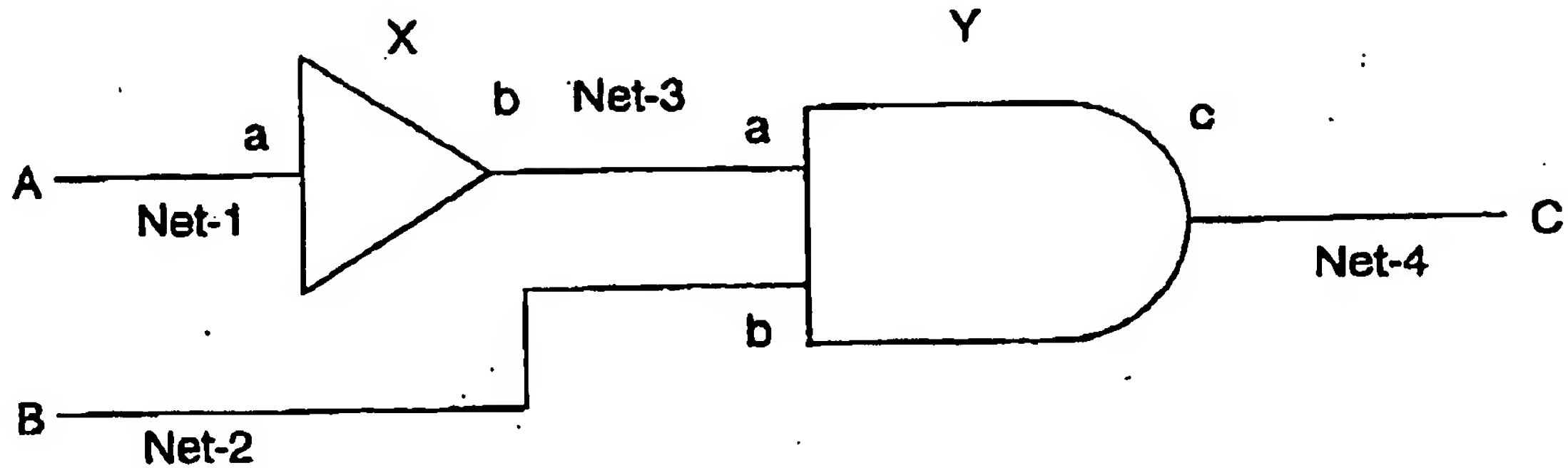(RAH) BUR920010207US1
1/4

10

Figure 1 (Prior Art)

BUR920010207US1
2/4

EXAMPLE OF LOGIC CIRCUIT

Figure 2 (Prior Art)

Port:
    INPUT : A, B:
    OUTPUT: C
EndPort
Net:
    Net-1: pA, Xpa;
    Net-2: pB, Ypb;
    Net-3: Xpb, Ypa;
    Net-4; pC, Ypc;
EndNet;

EXAMPLE OF NET LIST

Figure 3 (Prior Art)